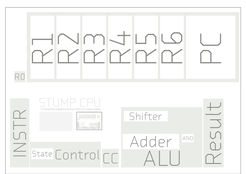
STUMP CPU

A Simplified Implementation With All Gates Visible

An implementation of the STUMP CPU from Manchester University's VLSI course. In this diagram every gate and every wire of every bus is shown. Obviously, this is not an example of good technique; in fact it aims to show the conciquences of not abstracting away details.

This design is likely to be slow and use more hardware than it should. It was designed purely with aesthetic appeal in mind.

Roughly 3,200 gates were used in this diagram (many more if simplified to only NAND gates).

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